WHAT IS CLAIMED IS:

1. A semiconductor memory device having a logic and a memory and selectively performing a late write operation and a boundary scan test operation, comprising:

a terminal receiving write data;

an input buffer provided corresponding to said terminal;

a boundary scan cell provided corresponding to said terminal and including a first register holding boundary scan test data at the time of said boundary scan test and holding write data to said memory supplied from said terminal at the time of said late write operation in accordance with inactivation of a write control signal;

a first selector receiving an output of said input buffer and an output of said boundary scan cell and selecting the output of said boundary scan cell in said late write operation; and

a write driver for writing the output selected by said selector into said memory.

2. The semiconductor memory device according to claim 1, wherein said boundary scan cell receives said boundary scan test data and the output of said input buffer, and said first register holds the output from said input buffer in said late write operation.

3. The semiconductor memory device according to claim 2, wherein said input buffer includes a latch circuit which holds the write data input from said terminal in an early write operation in accordance with activation of the write control signal and lets said write data through for output in said late write operation.

4. The semiconductor memory device according to claim 3, further comprising a control circuit which generates a one-shot pulse write data take-in signal in said early write operation based on a leading edge of a pulse of said write control signal and generates a one-shot pulse write data

take-in signal in said late write operation based on a trailing edge of a pulse of said write control signal, wherein

said boundary scan cell further includes

a second selector which receives an output of said input buffer, an input from said terminal and an output of a boundary scan cell in a preceding stage, and outputs the output of the boundary scan cell in the preceding stage in a shift operation of said boundary scan test, outputs the output of said input buffer in said late write operation, and outputs the input from said corresponding terminal at the time other than said shift operation and said late write operation, and

a logic gate which outputs said write data take-in signal in the late write operation, and outputs a clock signal for capturing and shifting of the boundary scan test in the capture and shift operations of the boundary scan test,

said first register latches an output of said second selector in accordance with an output of said logic gate, and outputs the same to a boundary scan cell in a succeeding stage and to said first selector, and

said first selector outputs the output of said input buffer in said early write operation and outputs the output of said boundary scan cell in said late write operation.

5. The semiconductor memory device according to claim 3, further comprising a control circuit which generates a one-shot pulse write data take-in signal in said early write operation based on a leading edge of a pulse of said write control signal and generates a one-shot pulse write data take-in signal in said late write operation based on a trailing edge of a pulse of said write control signal, wherein

said boundary scan cell further includes

a second selector which receives an input from said terminal and an output of a boundary scan cell in a preceding stage, and outputs the output of the boundary scan cell in the preceding stage in the shift operation of said boundary scan test, and outputs the input from said terminal at the time other than said shift operation,

a second register which latches an output of said second selector in accordance with a clock signal for capturing and shifting of said boundary scan test, and outputs the same to a boundary scan cell in a succeeding stage,

a third selector which receives an output of said input buffer and an output of said second register and outputs the output of said input buffer in said late write operation and outputs the output of said second register at the time other than said late write operation, and

a logic gate which outputs said write data take-in signal in the late write operation and outputs a clock signal for updating of the boundary scan test in the update operation of the boundary scan test,

said first register latches an output of said third selector in accordance with an output of said logic gate, and outputs the same to said first selector, and

said first selector outputs the output of said input buffer in said early write operation and outputs an output of said boundary scan cell in said late write operation.